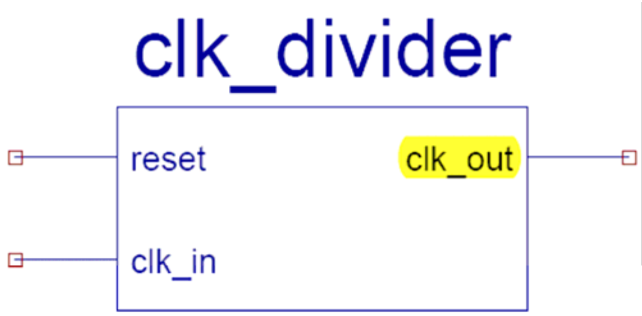
```
--------------------------------------------------------------------------------
-- Description:
--               In this top level module, two SRL16 (16-Bit Shift Register
--               Look-Up-Table) are cascaded to generate a clocks of 1MHz from
--               a system clock with much faster frequency range (3~80MHz)
--
--               By cascading more SRL16s, this clock divider can accept even
--               higher system frequency.
--
--               Each SRL16 only uses one LUT.
--------------------------------------------------------------------------------
```




```
generic ( CLK_DIV : integer range 0 to 15 := 12);
reset   : in  std_logic;    -- asynchronous reset
clk_in  : in  std_logic;    -- system clock
clk_out : out std_logic     -- output a slow clock

tmp <= CONV_STD_LOGIC_VECTOR(CLK_DIV,5); -- generate the address
addr <= tmp (3 downto 0);
d <= not q2;
clk_out <= clk_gen;
```